J. F. HOGG

IBM System/360 Model 67 Reference Data

FLOATING-POINT DOUBLE PRECISION INSTRUCTIONS

Load Mixed	LX	RX	R1, D2 (X2, B2)	74
Add Mixed Normalized	AX	RX	R1, D2 (X2, B2)	76
Add Double Normalized	ADDR	RR	R1, R2	26
Add Double Normalized	ADD	RX	R1, D2 (X2, B2)	66
Subtract Mixed Normalized	SX	RX	R1, D2 (X2, B2)	77
Subtract Double Normalized	SDDR	RR	R1, R2	27
Subtract Double Normalized	SDD	RX	R1, D2 (X2, B2)	67
Multiply Double Normalized	MDDR	RR	R1, R2	25
Multiply Double Normalized	MDD	RX	R1, D2 (X2, B2)	65
Store Rounded (Short)	STRE	RX	R1, D2 (X2, B2)	71
Store Rounded (Long)	STRD	RX	R1, D2 (X2, B2)	61

MODEL 67 INSTRUCTION CODES

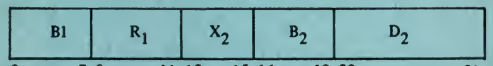
Instruction	Mnemonics	Type	Exceptions	Code
Load Multiple Control	LMC	RS	M, A, S, D, P	B8
Store Multiple Control	STMC	RS	M, P, A, S	B0
Load Real Address	LRA	RX	M, A, S	B1
Branch and Store	BASR	RR		0D
Branch and Store	BAS	RX		4D
Search List (RPQ)	SLT	RS	P, A, S, Reloc.	A2

Notes:

A	Addressing Exception
D	Data Exception
M	Privileged Operation Exception
P	Protection Exception
S	Specification Exception

LOAD REAL ADDRESS INSTRUCTION

LRA $R_1, D_2(X_2, B_2)$ [RX]

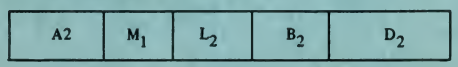


Resulting Condition Code:

0	Translation was successful
1	Translation unsuccessful (unavailability bit encountered in the segment table, or virtual address bits 0–7 > segment table register bits 0–7)
2	Translation unsuccessful (unavailability bit encountered in page table, or virtual address bits 12–19 > segment table entry bits 0–7)
3	---

When the resulting condition code is 1, the real address of the segment table entry is placed in the general register specified by R_1. When the resulting condition code is 2, the real address of the page table entry is placed in the general register specified by R_1.

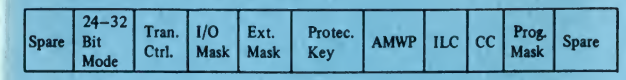
SEARCH LIST INSTRUCTION (RPQ)

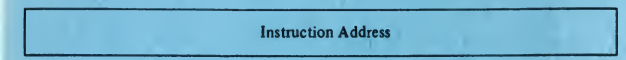


Resulting Condition Code:

0	Unsuccessful comparison or key test, completion due to count.
1	Successful comparison, unsuccessful key test.
2	Unsuccessful comparison, successful key test.
3	Successful comparison and key test.

EXTENDED PROG. STATUS WORD





Bit	Meaning	Bit	Meaning
0–3	Spare (must be 0 s)	15	Problem State (P)
4	24–32 Bit Address Mode	16–17	Instruction Length Code (ILC)
5	Translation Control	18–19	Condition Code (CC)
6	I/O Mask (Summary)	20–23	Program Mask:
7	External Mask (Summary)	20	Fixed Point Overflow Mask
8–11	Protection Key	21	Decimal Overflow Mask
12	ASCII-8 Mode (A)	22	Exponent Underflow Mask
13	Machine Check Mask (M)	23	Significance Mask
14	Wait State (W)	24–31	Spare
		32-63	Instruction Address

PSW Bit 13	Control Register 6 Bit 0	Bit 1	Remarks
0	x	x	Regardless of the status of bits 0 and 1 of control register 6, all machine checks are masked off by PSW bit 13.
1	0	0	Only CPU machine checks will be recognized.
1	0	1	CPU and Channel Controller 1 machine checks will be recognized.
1	1	0	CPU and Channel Controller 0 machine checks will be recognized.
1	1*	1*	All machine checks will be recognized.

*These bits are set to 1 by system reset. Program systems, other than TSS/360, that do not contain instructions for modifying control register 6 must use PSW bit 13 for control over machine check interruptions.

The following table summarizes the modes of operation:

Bit 4	Bit 5	Mode of Operation
0	0	No translation, except for LRA operand. 24–bit logical address (LRA only).
0	1	Translation for all program-generated addresses. 24–bit logical addressing.
1*	0	No translation, except for LRA operand. 32–bit logical addressing (LRA only).
1*	1	Translation for all program-generated addresses. 32–bit logical addressing.

*Specification exception if 32–bit option is not installed. The specification exception is recognized as part of the execution of the first instruction after the extended PSW is loaded.

CONTROL REGISTERS

Register	Bit Position Assignments	
0	Segment Table Register (for Dynamic Address Translation)	
1	Unassigned*	
2	Translation Exception Address Register	
3	Unassigned*	
4	Extended Mask Registers for I/O Channel Masks	
5	Unassigned*	
6	Bits 0, 1:	Machine Check Mask Extensions for Channel Controllers
	Bits 2, 3:	Reserved
	Bits 4-7:	Unassigned*
	Bit 8:	Extended Control Mode
	Bit 9:	Configuration Control Bit; defines when partitioning can take place.
	Bits 10–23:	Unassigned*
	Bits 24-31:	External interruption masking as follows:
	Bit Position	Interruption Source
	24	Timer
	25	Interrupt Key
	26	Malfunction Alert - CPU 1 (Ext. Sig. 2)
	27	Malfunction Alert - CPU 2 (Ext. Sig. 3)
	28	Reserved (Ext. Sig. 4)
	29	Reserved (Ext. Sig. 5)
	30	External Interrupt - CPU 1, 2 (Ext. Sig. 6)
	31	Reserved (Ext. Sig. 7)
7	Unassigned*	
8–14	Partitioning Sensing Registers. See 2167 description for register layout.	
15	Unassigned*	

*For expansion; not physically implemented.

INTERRUPT CODE LOCATIONS

In extended PSW mode, when the PSW is stored as the old PSW, the 16-bit interruption code is stored as a halfword in storage, as follows:

Interruption Type	Permanent Storage Address Decimal	Hex
External	14–15	E–F
SVC	16–17	10–11
Program	18–19	12–13
Machine check	20–21	14–15
I/O	22–23	16–17

These bytes are not loaded when loading a PSW.

2846 EXTERNAL MACHINE CHECK INTERRUPT CODES

		CABI			UABI							
		0	1	2	0	1	2	3	4	5	6	7
FAULT ↓ PSW Bits →	Note	21	22	23	24	25	26	27	28	29	30	31
									CPU			
Multiple CPU Recognition		0	0	0	1	0	0	0	1	2	3	4
									CABO			
CABO Parity Check		0	0	0	0	1	0	0	P	0	1	2
UABO Parity Check		0	0	0	0	0	1	0				
CABO and UABO Parity Checks		0	0	0	0	1	1	0				
						Channel						
Multiple Channel Recognition		1	1	0	0	0	1	2	3	4	5	6
										Stor ID		
Storage Interface Timeout	2, 4	1	0	0	0	1	0	0	0	4	2	1
										Chan ID		
Channel Interface Timeout	1	1	0	0	0	0	1	0	0	4	2	1
	1, 4		CSW	1		Prot						
SAB Parity Check	5	1	Store	1	0	Key	ID	SAB	Mark			
Invalid Address (CSW)	1, 6	1	1	1	0	0	0	0	0			
Multiple Storage Select	1, 4	1	0	0	0	0	0	1	0			
Multiple CCU Faults	3	1	--		1							
										Chan ID		
Prefix ID Parity Check						ID P	ID 1	ID 2	1	4	2	1

Note 1: The binary representation of the recognized channel is encoded.

Note 2: The binary representation of the selected storage unit is encoded. Storage A = 000, Storage B = 001, etc.

Note 3: PSW bits 22, 23, and 25-31 are ignored.

Note 4: 'Storage address check' signal returned to channel.

Note 5: Bit 22 set to 1 if any indicated check is detected during a CSW store operation.

Note 6: Invalid 'storage address check' signal always returned to channel. CCU external machine check interruption occurs only if channel is in a CSW store operation.

MACHINE CHECK INTERRUPTION

In addition to the machine check capability described in the IBM System/360 Principle of Operation manual, the 2067 performs machine checking on the dynamic address translation unit. Additional information about the machine check interruption is stored in the first byte (bits 0–7) of the translation exception address register (control register 2). Bits 50–54 in the maintenance control word indicate to the monitor whether a dynamic address translation unit machine check has caused the interruption; if it has, a 1-bit in the translation exception address register will indicate one of the following conditions:

Bit	Condition
0	More than one associative register contains identical information, or one of the comparing circuits is at fault.
1	A successful compare is achieved with a virtual address that is higher than the addresses in the segment table.
2	The virtual address portion of the translated address just stored in the associative array does not compare with the virtual address that should have been stored.
3	A reset of the load-valid bits in the associative array was unsuccessful.
4	Parity of the adder sum is inconsistent with the predicted parity.
5	Parity of the virtual address was incorrect when received by the associative array.
6	Parity of the data word from storage was incorrect when received by dynamic address translation circuitry.
7	Parity of instruction bits 8–15 was incorrect when received by dynamic address translation circuitry.

SYSTEM/360 MODEL 67 LIST OF INTERRUPTIONS

Interruption	Interruption Code (PSW Bits 16–31)	PSW Mask Bit STD	PSW Mask Bit EXT	ILC	How Instruction Execution Is Finished
Machine Check	00000000 00000000	13	13	u	Terminated
External machine check Mod. 2067-2 (see note 3)	10uuuuuu uuuuuuuu	13	13	u	Completed
Program					
Operation	00000000 00000001	–	–	1, 2, 3	Suppressed
Privileged operation	00000000 00000010	–	–	1, 2	Suppressed
Execute	00000000 00000011	–	–	2	Suppressed
Protection	00000000 00000100	–	–	0, 2, 3	Suppressed/Terminated
Addressing	00000000 00000101	–	–	1, 2, 3	Suppressed/Terminated
Specification	00000000 00000110	–	–	1, 2, 3	Suppressed
Data	00000000 00000111	–	–	2, 3	Suppressed/Terminated
Fixed-point overflow	00000000 00001000	36	20	1, 2	Completed
Fixed-point divide	00000000 00001001	–	–	1, 2	Suppressed/Terminated
Decimal overflow	00000000 00001010	37	21	3	Completed
Decimal divide	00000000 00001011	–	–	3	Suppressed
Exponent overflow	00000000 00001100	–	–	1, 2	Terminated
Exponent underflow	00000000 00001101	38	22	1, 2	Completed
Significance	00000000 00001110	39	23	1, 2	Completed
Floating-point divide	00000000 00001111	–	–	1, 2	Suppressed
Segment relocation	00000000 00010000	–	–	u	Suppressed
Page relocation	00000000 00010001	–	–	u	Suppressed
Supervisor Call	00000000 rrrrrrrr	–	–	1	Suppressed
External					
External signal 7	00000000 uuuuuuu1	7	7	u	Completed
External signal 6	00000000 uuuuuu1u	7	7	u	Completed
External signal 5	00000000 uuuuu1uu	7	7	u	Completed
External signal 4	00000000 uuuu1uuu	7	7	u	Completed
External signal 3	00000000 uuu1uuuu	7	7	u	Completed
External signal 2	00000000 uu1uuuuu	7	7	u	Completed
INTERRUPT pushbutton	00000000 u1uuuuuu	7	7	u	Completed
Timer	00000000 1uuuuuuu	7	7	u	Completed
I/O Mod. 2067-1					
Multiplexor channel	00000000 aaaaaaaa	0		u	Completed
Selector channel 1	00000001 aaaaaaaa	1		u	Completed
Selector channel 2	00000010 aaaaaaaa	2		u	Completed
Selector channel 3	00000011 aaaaaaaa	3		u	Completed
Selector channel 4	00000100 aaaaaaaa	4		u	Completed
Selector channel 5	00000101 aaaaaaaa	5		u	Completed
Selector channel 6	00000110 aaaaaaaa	6		u	Completed
I/O – Mod. 2067-2 (see note 5)					
CCU 1	0000bbbb aaaaaaaa		6	u	Completed
CCU 2	0001bbbb aaaaaaaa		6	u	Completed
CCU 3	0010bbbb aaaaaaaa		6	u	Completed
CCU 4	0011bbbb aaaaaaaa		6	u	Completed

1) The following abbreviations are used in table:
   - u - unpredictable
   - r - R1 and R2 fields in Supervisor Call instruction
   - a - I/O device address
   - b - I/O channel address

2) When an interruption occurs in standard PSW mode, interruption code is stored in bits 16–31 of old PSW. When an interruption occurs in extended PSW mode, the interruption code is stored in locations 00E–017.

3) In extended PSW mode, bit 13 is the overall machine check interrupt mask and includes external machine check interrupts. If PSW (13) = 0, all machine check interrupts are masked off. When PSW (13) = 1, all machine check interrupts are taken. The external machine check interrupts are treated individually according to their associated mask bits contained in CPU control register 4.

4) Extended PSW bit 7 is the overall external interrupt mask. If PSW (7) = 0, all external interrupts are masked off. If PSW (7) = 1, external interruptions are treated individually according to their associated mask bits in CPU control register 6.

5) Extended PSW bit 6 is the overall I/O interruption mask. If PSW (6) = 0, all I/O channels are masked off. If PSW (6) = 1, I/O interrupts are treated individually according to their associated mask bits in CPU control registers 4 and 5.

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PROGRAM INTERRUPTS - DAT

CODE	TYPE	CAUSE
6	Specification	Page table reg bits 13–15 not zero
7	Data	Segment table register bits 26–31 not zero
16	Segment (ABO) Relocation	Logical address bits 0–7 greater than STR bits 0–7 or segment table entry (STE) unavailable (bit 31 = 1)
17	Page (ABO) Relocation	Logical address bits 12–19 greater than segment table* entry bits 0–7 or page table entry (PTE) unavailable – bit 12 (or 28) = 1 (½word position 12) and zeros in 13–15.

*Entry in page table reg

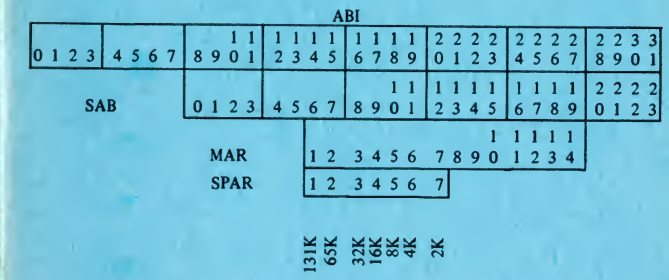
EXTENDED DIRECT CONTROL

Interrupt Line	CPU 1	CPU 2
2	Not used	Machine check out signal from CPU 1
3	Machine check out signal from CPU 2	Not used
4, 5	Reserved for future use	
6	Timing signal from CPU 1 or CPU 2	Timing signal from CPU 1 or CPU 2
7	Not used	Not used

Line numbers correspond to external signal designations used with the interruption codes listed in the IBM System/360 Principles of Operation manual. Interrupt codes and mask bits for these lines are as follows:

Line	Control Register 6 External Interrupt Mask Bit	Interruption Code
2	26	00000000 nnlnnnnn
3	27	00000000 nnnlnnnn
6	30	00000000 nnnnnnln

STORAGE ADDRESSING



SAB BITS 4 5

0 0 = 2365 # 1
0 1 = 2365 # 2
1 0 = 2365 # 3
1 1 = 2365 # 4

SENSE BYTES

BYTE 0

Bit / Device	0	1	2	3	4	5	6	7
1052, 2150	Cmd Rej	Int Req	Bus Out	Eq Chk				
2540/ 1821	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk		Unusual Cmd	
1403 1443	Cmd Rej	Int Req	Bus Out	Eq Chk	Type Bar	Type Bar		Ch 9
1442, 2501 2520	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Over-run		
2671/ 2822	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk			
2400	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Over-run	Wrt Cnt Zero	Data Convtt Chk
2311/ 2841	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Over-run	Trk Ccnd Chk	Seek Chk
2301/ 2820	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Over-run		Inval Addr
2250	Cmd Rej	Should Not Occur	Bus Out	Should Not Occur	Data Chk	Should Not Occur	Buffer Run-ning	Should Not Occur
2260	Cmd Rej	Int Req	Bus Out	Eq Chk	Should Not Occur	Should Not Occur	Should Not Occur	Should Not Occur
2280	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Should Not Occur	Should Not Occur	Illgl Seg
2282	Cmd Rej	Int Req	Bus Out	Eq Chk	Data Chk	Should Not Occur	Should Not Occur	Illgl Segn

SENSE BYTES

BYTE 1

Bit / Device	0	1	2	3	4	5	6	7
2400	Noise	00-Non-Xst Tu 01-Not Ready 10-Rdy & No Rwd 11-Rdy & Rwdng		7 Trk	At Load Point	Wrt Status	File Protect	Tape Ind
2311/ 2841	Data Chk Fld	Trk Over-run	End of Ctl	Invalid Seq	No Rec Found	File Prot	Missing Addr Mrkr	Over-Flow Inl
2301/ 2820	Data Chk In Count	Trk Over-run	End of Cyl.	Inval Seq	No Rec Found	File Prot	Service Over-run	Over-Flow Inl
2250	Light Pen Detect	End Order Seq	Char Mode					
2280	Read Count Chk	Film Low	Recrdr Forced Gap	Should Not Occur	Should Not Occur	2840 Output Chk	2840 Input Chk	Graphic Chk
2282	Read Count Chk	Film Low	Recrdr Forced Gap	Film Motion Limit	Should Not Occur	2840 Output Chk	2840 Input Chk	Graphic Chk

BYTE 2

Bit / Device	0	1	2	3	4	5	6	7
2400	Bits 0 – 7 indicate a track is in error						6 & 7 indicate no error or multi-error	
2311/ 2841	Un-safe		Serial-izer Chk	Tag Line Chk	Alu Chk	Unsel Status		
2301/ 2820	Un-safe	Shift Reg	Skew Fail	Ctr Chk	Comp Chk			
2250		Buffer Address Register Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
2280		Buffer Address Register Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
2282		Buffer Address Register Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9

SENSE BYTES

BYTE 3

Bit / Device	0	1	2	3	4	5	6	7
2400	R/W Vrc	Lrcr	Skew	Crc	Skew Req Vrc	DE	Bkwd Status	Com-pare
2311/ 2841	Ready	On Line	Read Safety	Write Safety		End of Cyl		Seek Incmpl
2301/ 2820	Lrc Bit 0	Lrc Bit 1	Lrc Bit 2	Lrc Bit 3				
2250	Buffer Address Register Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
2280	Buffer Address Register Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
2282	Buffer Address Register Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1

BYTE 4

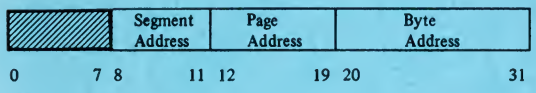
2400	Echo Err	Res Tape Unit	Read Clock Err	Write Clock Err	Delay Counter Err	Seq Ind C	Seq Ind B	Seq Ind A
2301/ 2820	Seq Ind 0	Seq Ind 1	Seq Ind 2	Seq Ind 3	Seq Ind 4	Seq Ind 5	Seq Ind 6	Seq Ind 7

BYTE 5

2311/ 2841	Command In Progress When Overflow Incomplete Occurs. or Zero
2301/ 2820	Command In Progress When Overflow Incomplete Occurs. Write = X'05' or Read = X'06' Zero

VIRTUAL ADDRESS

The virtual address operand is formed from the base address, index, and/or displacement as determined by the instruction format. The resulting virtual operand address has three parts:



FORMAT OF REGISTERS AND ENTRIES

Bits	Meaning	Remarks
1. Segment Table Register Format:		
0–7	Segment Table Length*	Indicates the number of 16-entry groups in the segment table. All zero = One group.
8–31	Segment Table Origin	Since the segment table origin is located on a 64-byte boundary, bits 26–31 must be zero.
2. Segment Table Entry Format:		
0–7	Page Table Length	Indicates the number of entries in the page table. All zero = One entry.
8–30	Page Table Origin	The page table origin is located on a 2-byte boundary.
31	Page Table Availability	1 = Segment translation exception (program interrupt code 16).
3. Page Table Entry (Halfword):		
0–11	Physical Block Address	Starting addresses of page.
12	Page Availability	1 = Page translation exception (program interrupt code 17).
13–15	Control Bits, Reserved	Must be 000 or specification exception.

*Used only with CPU's that contain the 32-bit addressing feature.

ASSOCIATIVE REGISTER FORMAT

24-Bit Addressing:

Bits	Content	Remarks
8–19	Virtual Address	
20–31	Physical Address	The page address from a previous translation which corresponds to the virtual address in bit 8–19.
32–35	Unassigned *	
36	Register Valid	Set to 1 upon loading the register.
37	Recent Usage - "Load"	Set to 1 upon loading the register and upon any use thereafter.
38	Disable	Set with special diagnose codes 8–15.

32-Bit Addressing: Same as above except for virtual address, which is in bits 0–19.

*For expansion, not physically implemented.

BIT ALIGNMENT OF ADDRESS ARITHMETIC

1. Segment Table Entry Address

Bits (24-Bit Mode)	Meaning	Remarks
8–31	Table Origin	Bits 26–31 are considered zero.
8–11	Added to Logical Address	Aligned with 26–29 of segment table origin.
8–31	Yields Sum	Segment table entry address (30–31 always zero).

Bits (32-Bit Mode)	Meaning	Remarks
8–31	Table Origin	26–31 are considered zero.
0–11	Added to Logical Address	Aligned with 18–29 of segment table origin.
8–31	Yields Sum	Segment table entry address (30–31 always zero).

2. Page Table Entry Address - Either 24- or 32-Bit Mode

Bits	Meaning	Remarks
8–31	Page Table Origin	31 is considered zero.
12–19	Added to Logical Address	Aligned with 23–30 of page table origin.
8–31	Yields Sum	Page table entry address (31 is always zero.)

3. Physical Address Result

Bits	Meaning	Remarks
0–11	Page Table Entry	The high-order portion.
20–31	Logical Address	The low-order portion.
8–31	Physical Address	Both portion taken together.